PATENT ABSTRACTS OF JAPAN

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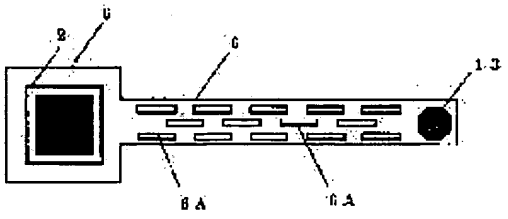
(72)Inventor : TAKAO YUKIHIRO
SHINOKI HIROYUKI

(54) CHIP-SIZED PACKAGE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To effectively relax a stress in a Cu wiring by a method, wherein a plurality of slips provided in a wiring layer are rectangular and the long sides of the slits are properly arranged in the direction where the wiring layer is provided extendedly.
SOLUTION: A plurality of slits 6A are provided in a Cu wiring layer 6, the slits 6A are rectangular, the long sides of the slits 6A are arranged in such a way as to extend along the direction where the layer 6 is extendedly provided and the slits 6A are alternately arranged, whereby the slits are uniformly arranged, and the effect to relax stress in a Cu wiring can be increased. The width of the layer 6 is 50 to 100 μm, taking into consideration the current capacity and mechanical strength and the size of the slits is restricted by the processing accuracy of a photoresist, which is used in an electrolyte plating, but the length (the long sides) of the slits is 90 nm, the width (the short sides of the slits) of the slits is 10 μm and the distance between the adjacent slits is 10 μm or thereabouts. Accordingly, by providing the plurality of the slits in the Cu wiring layer, the stress in a Cu wiring is relaxed, and the deterioration of the characteristics of a transistor directly under the wiring layer can be prevented.



LEGAL STATUS

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[Date of final disposal for application]

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The chip-size package characterized by preparing two or more slits in the aforementioned wiring layer in the chip-size package possessing the wiring layer which consists of Cu which is connected to a metal-electrode pad and extends on a chip front face, the insulating layer which covers the chip front face containing this wiring layer, opening formed in the insulating layer on the aforementioned wiring layer, and the pillar-shaped terminal formed in this opening.
[Claim 2] The chip-size package characterized by preparing two or more slits at the aforementioned wiring layer in the chip-size package possessing two or more wiring layers which consist of Cu which connects two or more metal-electrode pads arranged around an LSI chip, two or more pillar-shaped terminals arranged in the shape of an array on an LSI chip, this pillar-shaped terminal, and the aforementioned metal-electrode pad.
[Claim 3] Two or more aforementioned slits are chip-size packages according to claim 1 or 2 which are a rectangle and are characterized by arranging the long side in the extension direction of the aforementioned wiring layer.
[Claim 4] The wiring layer which consists of Cu which is connected to a metal-electrode pad and extends on a chip front face. The insulating layer which covers the chip front face containing this wiring layer. Opening formed in the insulating layer on the aforementioned wiring layer. The pillar-shaped terminal formed in this opening. It is the manufacture method of the chip-size package equipped with the above, and in the process which forms the aforementioned wiring layer, after forming a photoresist layer on the field except the schedule field which forms this wiring layer, and the schedule field which prepares a slit on a wiring layer, it is characterized by performing electrolysis plating.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to a chip-size package and its manufacture method. It is referred to also as CSP, and a chip-size package (Chip Size Package) is equivalent to a chip size, or is the general term of a slightly large package, and is a package aiming at high density assembly. this invention relates to the technology which raises the reliability of a chip-size package.
[0002]
[Description of the Prior Art] Conventionally, generally it is referred to as BGA (Ball Grid Array), and is called structure and the fine pitch BGA with two or more pewter balls arranged in the shape of a field, and the structure from which the ball pitch of BGA was further made into the ** pitch, and the PKG appearance became a chip size closely is known for this field.
[0003] Moreover, recently, it is the "Nikkei micro device" August, 1998 issue. There is a wafer CSP indicated by 44 pages - 71 pages. Fundamentally, this wafer CSP is CSP which makes the pad of the shape of wiring or an array from a wafer process (last process) before the dicing of a chip. It is expected that a wafer process and a package process (back process) are unified, and package cost can decrease now sharply with this technology.
[0004] There are a closure plastic pattern and a rewiring type in the kind of wafer CSP. A closure plastic pattern is the structure which was wearing the front face by the closure resin like the conventional package, and is the structure of forming a pillar-shaped terminal (metal post) on the wiring layer on the front face of a chip, and hardening the circumference by the closure resin. If a package is carried in a printed circuit board, the stress generated by the differential thermal expansion with a printed circuit board will concentrate on a metal post. Generally, it is known that stress will be distributed, so that this metal post is lengthened.
[0005] On the other hand, a rewiring type is drawing. It is the structure which did not use a closure resin but formed rewiring so that it may be shown. The laminating of the aluminum electrode 52, a wiring layer 53, and the insulating layer 54 is carried out to the front face of a chip 51, the metal post 55 is formed on a wiring layer 53, and the solder bump 56 is formed on it. A wiring layer 53 is used as rewiring for stationing the solder bump 56 in the shape of [predetermined] an array on a chip.
[0006]
[Problem(s) to be Solved by the Invention] As mentioned above, generally in a chip-size package, aluminum electrode pad 52 arranged at the rim of an LSI chip and the metal post 55 (pillar-shaped terminal) regularly arranged in the shape of an array are connected with Cu (copper) wiring.
[0007] However, although the coefficient of linear expansion of Cu is equivalent (Cu:20ppm, aluminum:29ppm) with aluminum, in Young's modulus, it is twice [about] (Cu:12.98x1010, aluminum:7.03x1010) the aluminum.

[0008] For this reason, under environment, such as a heat cycle test at the time of CSP mounting, Cu wiring is multiplied by the metal post 55, gives a big stress to the transistor of LSI which is directly under it, and has the concern which degrades transistor characteristics.

[0009]

[Means for Solving the Problem] In order that the chip-size package and its manufacture method of this invention might be made in view of the above-mentioned technical problem and might ease the stress (stress) of Cu wiring, two or more slits were prepared in the wiring layer. These slits are rectangles and can ease stress effectively by arranging the long side in the extension direction of the aforementioned wiring layer.

[0010]

[Embodiments of the Invention] Next, the operation gestalt of this invention is explained, referring to drawing 1 or drawing 10 .

[0011] Drawing 1 is the flat surface of a chip-size package. Two or more aluminum electrode pads 2 of LSI are arranged at the periphery on a chip. And two or more pillar-shaped terminals 13 (metal post) are regularly arranged in the shape of an array in the field surrounded with aluminum electrode pad 2. A solder ball may be installed on these pillar-shaped terminals 13. Furthermore, in order to wire between these aluminum electrode pads 2 and pillar-shaped terminals 13, the wiring layer 6 which consists of Cu (**) has extended the chip top. In addition, as shown in drawing, all the pillar-shaped terminals 13 are not wired, only the required pillar-shaped terminal 13 is chosen, and wiring is made.

[0012] Drawing 2 is the enlarged view of the portion surrounded with the dashed line in drawing 1 . That is, it is the plan to which 1 set of aluminum electrode pads 2, the wiring layer 6, and the pillar-shaped terminal 13 were expanded. Two or more slit 6A (hole prepared in the wiring layer) is prepared in the wiring layer 6.

[0013] Slit 6A is a rectangle, and it has arranged the long side so that it may meet in the extension direction of a wiring layer. Moreover, by arranging by turns, a slit can be arranged uniformly and can increase a stress relaxation effect.

[0014] The width of face of a wiring layer 6 is 50 micrometers - 100 micrometers, when current capacity and a mechanical strength are taken into consideration. although the size of a slit receives restrictions by the process tolerance of the photoresist used by electrolysis plating explained later -- length (long side): -- 90 micrometers of distance between the slits which adjoin width-of-face (shorter side):10micro are about 10micro

[0015] Next, the manufacture method of the chip-size package of this invention is explained, referring to drawing 3 or drawing 10 .

[0016] First, as shown in drawing 3 , the semiconductor substrate 1 (wafer) in which LSI which has aluminum electrode pad 2 was formed is prepared, and the front face of the semiconductor substrate 1 is covered with the passivation films 3, such as a SiN film.

[0017] aluminum electrode pad 2 is a pad for external connection of LSI. The passivation film 3 of the front face is removed by etching, and the barrier metal 4 is formed in the whole surface. The barrier metal 4 is barrier which intervenes between the wiring layers and aluminum electrode pads 2 which are formed behind, and protects aluminum electrode pad 2, carries out the spatter of chromium (Cr), the titanium (Ti), etc., and forms them.

[0018] Next, the wiring layer 6 linked to aluminum electrode pad 2 is formed. It is appropriate for this wiring layer 6 for it to be necessary to form in about 5 micrometers thickly, in order to secure a mechanical strength, and to form using electrolysis plating.

[0019] As shown in drawing 4 , the photoresist layer 5 is formed in the field except the schedule field which is on the barrier metal 4 and forms a wiring layer 6. The photoresist layer 5 is formed also in

the schedule field which forms slit 6A on a wiring layer 6 at this time.

[0020] And it uses as an electrode of plating of the barrier metal 4, and the wiring layer 6 which consists of a deposit of Cu is formed on the barrier metal 4 which is not covered in the photoresist layer 5. At this time, slit 6A is simultaneously formed on a wiring layer 6.

[0021] Then, the photoresist layer 5 is removed, further, it etches using a wiring layer 6 as a mask, and the garbage of the barrier metal 4 is removed.

[0022] Next, as shown in drawing 5 , the 1st polyimide layer 7 is applied to the whole surface, and the 1st opening 8 is formed in the 1st polyimide layer 7 on a wiring layer 6 by exposure and development. It is desirable to use a highly sensitive negative system polyimide as 1st polyimide layer 7. The thickness is 20 micrometers - 25 micrometers at the maximum. The diameter of opening of the 1st opening 8 has good about 50 micrometers.

[0023] Moreover, as for after development, it is good to bake the 1st polyimide layer under the temperature of about 200 degrees C. This is for preventing mixing with the 2nd polyimide layer formed at the following process.

[0024] Subsequently, as shown in drawing 6 , the 2nd polyimide layer 9 is applied to the whole surface. It is desirable that this 2nd polyimide layer 9 also uses a negative system polyimide. The thickness is 20 micrometers - 25 micrometers at the maximum like the 1st polyimide layer 7. The 1st opening 8 is filled by the 2nd polyimide layer 9. Next, as shown in drawing 7 , the 2nd opening 10 is formed on the 1st opening 8 by exposing and developing the 2nd polyimide layer 9. The 2nd opening 10 is formed in the position which laps with the 1st opening 8 superficially, the polyimide filled by the 1st opening 8 is also removed, and the front face of a wiring layer 6 is exposed. Here, if a negative system polyimide is used as 2nd polyimide layer, the exposure field will turn into a field except the 2nd opening 10. And after development, in the exposed field, the 2nd polyimide layer 9 hardened by exposure remains, and the polyimide of the field used as the 2nd opening 10 is removed in response to an operation of a developer to it. Thus, what is necessary is not to expose the thick polyimide layer filled by the 1st opening 8 to the lower layer, and just to expose the polyimide layer which has the original thickness applied on the flat part by using a negative system polyimide. Thereby, even if it applies the 2nd 20 micrometers - 25 micrometers thick polyimide layer 9, the 2nd opening 10 can be formed.

[0025] Moreover, as for the edge of the 2nd opening 10, it is desirable that you make it separated and located outside the edge of the 1st opening 8. That is, a phot mask is designed so that delta (delta> 0) in drawing 5 may arise. Thereby, a hardening layer can be certainly formed over the whole polyimide by exposure, and poor resolving of a polyimide can be prevented.

[0026] Next, as shown in drawing 8 , the seed layer 11 for plating is formed in the whole surface. This seed layer serves as an electrode in the case of plating, can carry out the spatter of the Cu and can form it. And the photoresist layer 12 is formed on the seed layer 11. The photoresist layer 12 is processed by the phot lithography method so that it may have opening on the 1st, the 2nd opening 8, and 10.

[0027] Next, as shown in drawing 9 , the metal post 13 as a pillar-shaped terminal which consists of Cu by electrolysis plating, the barrier layer 14, and the solder bump 15 are formed one by one. the barrier property to the solder bump who contains Pb and Sn as a barrier layer 14 -- taking into consideration -- the metal of Pt system, for example, Au and nickel, -- it is good to use the cascade screen of these

[0028] Finally, as shown in drawing 10 , the photoresist layer 12 is removed and etching removes the garbage of the seed layer 11 by using the solder bump 15 as a mask. And according to a dicing process, the semiconductor substrate 1 is divided into a chip along with a scribe line, and is completed as a chip-size package.

[0029] Thus, the polyimide layer of the impasto of 40 micrometers - 50 micrometers can be formed by using a negative system polyimide. Consequently, it can form for a long time with 40 micrometers - 50 micrometers, the stress concerning a metal post is eased also in the chip-size package which does not use a closure resin, and a metal post can also improve reliability.
[0030]
[Effect of the Invention] According to the chip-size package of this invention, by preparing two or more slits in Cu wiring layer, stress (stress) can be eased and property degradation of a transistor [directly under] can be prevented.
[0031] Moreover, according to the manufacture method of the chip-size package of this invention, two or more slits can be prepared simultaneously with formation of Cu wiring layer with electrolysis plating.

[Translation done.]

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TECHNICAL FIELD

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PRIOR ART

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MEANS

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[0023] Moreover, as for after development, it is good to bake the 1st polyimide layer under the temperature of about 200 degrees C. This is for preventing mixing with the 2nd polyimide layer formed at the following process.

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[0028] Finally, as shown in drawing 10 , the photoresist layer 12 is removed and etching removes the garbage of the seed layer 11 by using the solder bump 15 as a mask. And according to a dicing process, the semiconductor substrate 1 is divided into a chip along with a scribe line, and is completed as a chip-size package.

[0029] Thus, the polyimide layer of the impasto of 40 micrometers - 50 micrometers can be formed by using a negative system polyimide. Consequently, it can form for a long time with 40 micrometers - 50 micrometers, the stress concerning a metal post is eased also in the chip-size package which does not use a closure resin, and a metal post can also improve reliability.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the plan showing the chip-size package concerning the operation gestalt of this invention.
[Drawing 2] It is the plan showing the chip-size package concerning the operation gestalt of this invention.
[Drawing 3] It is the 1st cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 4] It is the 2nd cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 5] It is the 3rd cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 6] It is the 4th cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 7] It is the 5th cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 8] It is the 6th cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 9] It is the 7th cross section showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 10] It is the cross section of the octavus showing the manufacture method of the chip-size package concerning the operation gestalt of this invention.
[Drawing 11] It is the cross section showing the chip-size package concerning the conventional example.

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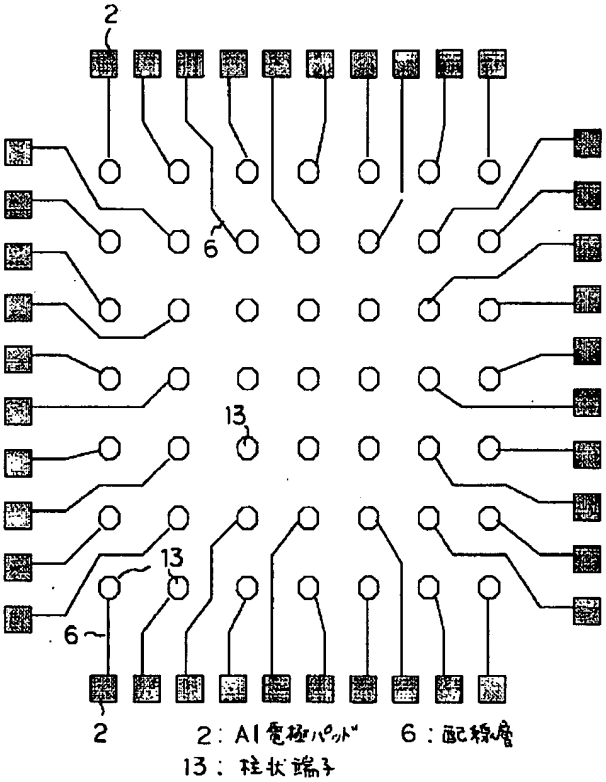
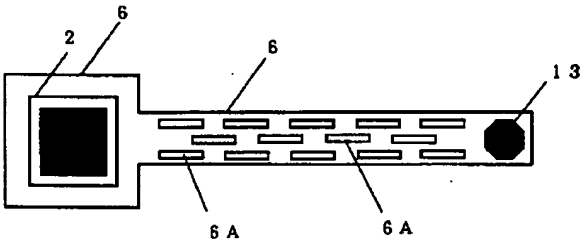
DRAWINGS

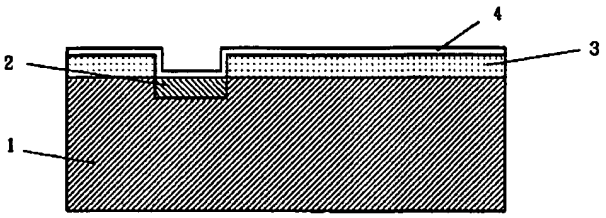
[Drawing 1]



[Drawing 2]

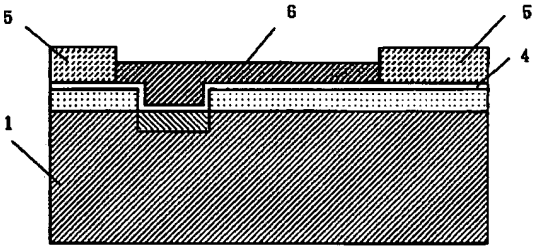


[Drawing 3]



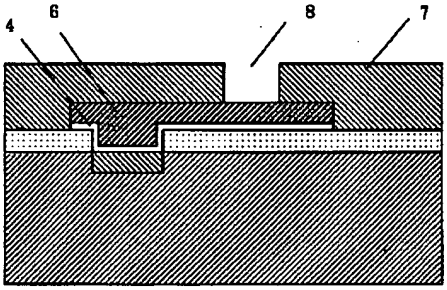
1：半導体基板　　2：Ａｌ電極パッド
3：パッシベーション膜　4：バリアメタル

[Drawing 4]



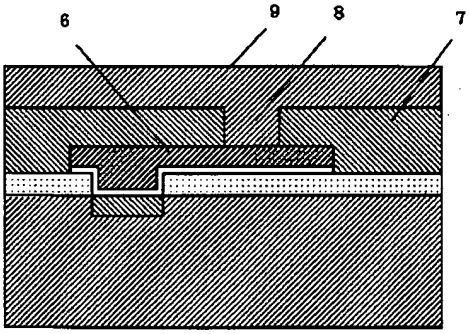
5：ホトレジスト層
6：配線層

[Drawing 5]



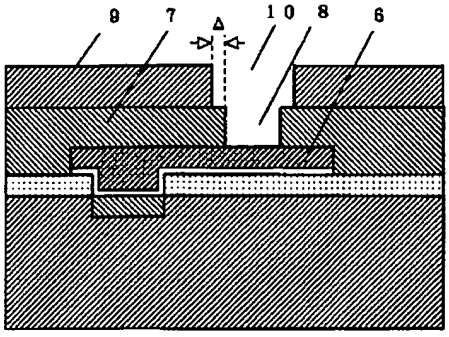
7：第１のポリイミド層
8：第１の開口部

[Drawing 6]



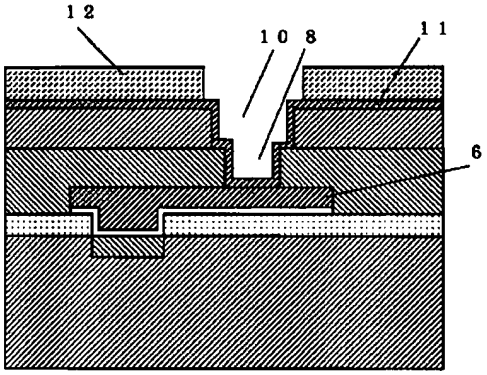
9：第２のポリイミド層

[Drawing 7]



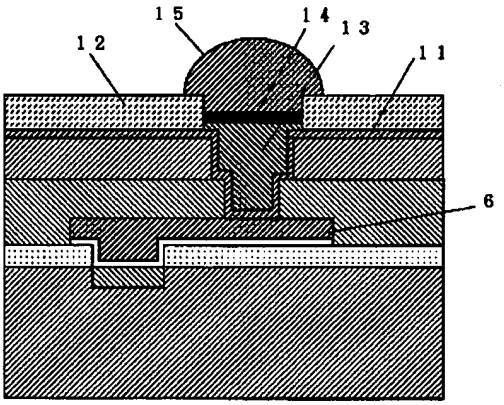
１０：第２の開口部

[Drawing 8]



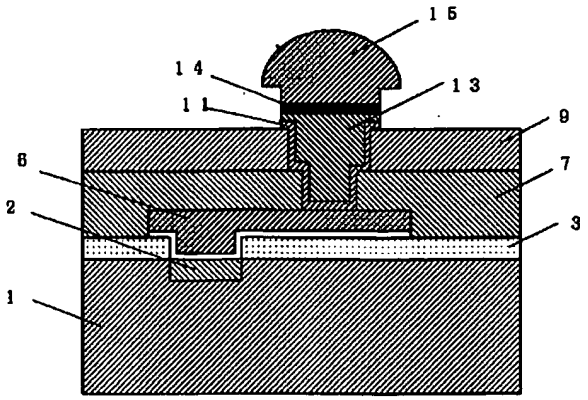
１１：シード層
１２：ホトレジスト層

[Drawing 9]

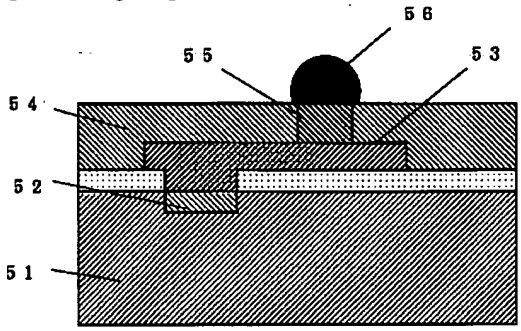


１３：メタル・ポスト
１４：バリア層　　１５：半田バンプ

[Drawing 10]



[Drawing 11]



51：チップ	54：絶縁層
52：Al電極	55：メタル・ポスト
53：絶縁層	56：半田バンプ

[Translation done.]